REMARKS

In the present application, claims 1-44 are pending. Claims 1-44 were rejected. Claim 2 has been amended. No new matter has been added. As a result of this response, claims 1-44 are believed to be in condition for allowance.

Claim Objections

The Examiner objected to claims 2 because of an informality. Claim 2 is amended herein in accordance with the Examiner's requirement to correct. As a result, Applicants respectfully traverse the objection to claim 2.

Claim Rejections – 35 USC § 102(e)

The Examiner rejected claims 1-4, 6-16, 18, 22-25, 27-36, 39, and 43-44 as being anticipated by Christie (6,877,084).

The Examiner rejected claim 1 asserting that Christie "discloses a digital data processor (See column 4, lines 59-63) comprising an instruction unit (See column 5, lines 34-44), said instruction unit comprising a code page (See column 7, lines 36-45: Ability to page indicates a code page) that is partitioned for storing in a first section thereof a plurality of instruction words (See figure 7: Standard Register Set 84) and, in association with at least one instruction word, in a second section thereof an extension to said at least one instruction word (See figure 7: Extended Register Set).

Applicants respectfully disagree with the Examiner's characterization of the disclosure of Christie. Specifically, Applicants assert that Christie does not disclose a code page as recited. Furthermore, Christie does not disclose any entity or element for storing in a first section a plurality of instruction words and an extension to at least one of the instruction words in a second section.

Claim 1 recites:

1. A digital data processor comprising an instruction unit, said instruction unit

comprising a code page that is partitioned for storing in a first section thereof a plurality of instruction words and, in association with at least one instruction word, in a second section thereof an extension to said at least one instruction word.

The Examiner cited column 7, lines 36-45 and the Standard Register Set 84 and Extended Register Set of Fig. 7 as disclosing the claimed code page "partitioned for storing in a first section thereof a plurality of instruction words and, in association with at least one instruction word, in a second section thereof an extension to said at least one instruction word". In fact, Christie discloses no such thing. At column 7, lines 36-45 Christie states:

> Referring back to FIG. 5, it is noted that CPU 32 may also include a memory management unit having paging hardware to implement paging address translation from virtual addresses to physical addresses. A "virtual address" is an address generated prior to translation via an address translation mechanism (e.g. a paging mechanism) to a "physical address", which is the address actually used to access a memory. The paging hardware may include a translation lookaside buffer (TLB) to store page translations.

As is evident, Christie describes a memory management unit having hardware for translating between virtual addresses and physical addresses for use in accessing memory. As Christie further describes at col. 7, lines 59-67:

> Execution core 52 executes instructions fetched from instruction cache 50. Execution core 52 obtains register operands from register file 60, and stores register result values within register file 60. The size of operands is dependent upon the operating mode of CPU 32, and may be overridden by instructions as described below. Execution core 52 obtains memory operands from data cache 54, and provides memory result values to data cache 54 as described below.

As is further evident, the paging mechanism described above is used by the execution core to fetch instructions from instruction cache 50 and memory operands from data cache 54. As described further at col. 8, lines 52-56, "Data cache 54 may provide the memory operand

addresses to paging hardware within the memory management unit for translation from virtual addresses to physical addresses." Thus, the disclosed paging mechanism can be used, generally, to obtain physical addresses in the memories formed by the instruction cache 50 and the data cache 54. Applicants assert that is common for memory to be formed of memory pages.

It is important to note, however, that there is no disclosure of using the paging mechanism to retrieve data from the register file that includes the standard register set and the extended register set. This observation arises from the fact that the standard register set and the extended register set do not form part of any memory formed of a memory page or pages. Rather, as disclosed by Christie at col. 3, lines 10-19, "The eight 32-bit general purpose registers may include, for example, the EAX, EBX, ECX, EDX, ESP, EBP, ESI, and EDI registers. The extended register set may include the eight 32-bit general purpose registers of the standard register set and eight additional 32-bit registers not defined by the x86 architecture." As is evident, the standard register set is formed of eight standard registers, each four bytes in size, that are referenced by name (or, in the alternative, by three bits of register operand identification information) – not by address. They form no part of a memory page and hence, their access is not facilitated through the use of any paging mechanism. Similarly, the extended register set is formed of eight additional registers not defined by the x86 architecture.

Combining the disclosures of Christie discussed above, it is clear that Christie fails to teach numerous elements recited in claim 1. First, despite the disclosure of a paging mechanism, there is no disclosure of an actual page, code or otherwise. As there is no disclosure of mention of a code page, there is, therefore, no mention of specific attributes of the code page recited in claim 1. Specifically, claim 1 recites that the code page is partitioned into a first section for storing a plurality of instruction words and a second section for storing in association with at least one instruction word an extension to the at least one instruction word. As noted above, because Christie does not disclose a page or code page, it does not disclose any such structure as recited in claim 1. Applicants further assert that Christie does not elsewhere, outside of the Examiner's citations, disclose any such code pages as claimed.

Second, while Christie does not disclose, in general, the claimed code pages, contrary

to the Examiner's assertions, the register sets of Christie most emphatically and specifically do not comprise first and second sections of any form of a page. Third, while the Examiner is incorrect in asserting that the register sets of Christie are equivalent to the claimed first and second sections of claim 1, it is further erroneous to assert, as the Examiner does, that the first register set and extended register set store instruction words and extensions to the instruction words, respectively. In fact, as discussed above, the registers of Christie are standard x86 general purpose registers and do not store instructions. In addition, while the registers of the extended register set extend the number of registers for use by the CPU, none of the extended registers form an extension to any one register in the standard register set.

For all of the reasons discussed above, claim 1 is in condition for allowance. As independent claims 22 and 43 recite elements similar to those discussed above with reference to claim 1, they are likewise in condition for allowance. As all of claims 2-4, 6-16, 18, 23-25, 27-36, 39, and 44 depend upon claims 1, 22 and 43, they are likewise in condition for allowance.

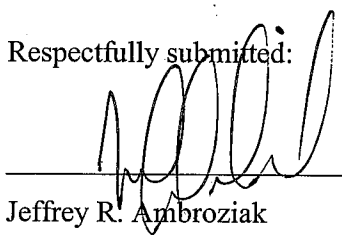
Claim Rejections – 35 USC § 103(a)

The Examiner rejected claims 5, 17, 19-21, 26, 38 and 40-42 as being unpatentable over Christie in view of Yates et al. (6,397,379 B1).

With respect to all of the claims rejected under 35 USC § 103(a), Applicants respectfully note that they are dependent upon independent claims 1, 22, and 43. As the disclosure of Yates does not cure the deficiencies in Christie described above, nor does the Examiner assert that it does, all of claims 5, 17, 19-21, 26, 38 and 40-42 are likewise in condition for allowance.

The Examiner is respectfully requested to reconsider and remove the rejections of the claims, and to allow all of the pending claims 1-44 as now presented for examination. An early notification of the allowability of the pending claims is earnestly solicited.

Respectfully submitted:



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